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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,767	08/13/2001	Khushrav S. Chhor	5732-00100 MD-080	7633

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EXAMINER	
FUREMAN, JARED	

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,767	CHHOR ET AL.	
	Examiner	Art Unit	
	Jared J. Fureman	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the amendment, filed on 12/8/2003, and the IDS, filed on 12/17/2003, all of which have been entered in the file. Claims 1-27 are pending.

Drawings

1. The drawings were received on 12/8/2003. These drawings are acceptable.

Claim Objections

2. Claim 2 is objected to because of the following informalities: Claim 2, line 1: "the" (second occurrence) should replaced with --an--, in order to avoid a lack of proper antecedent basis for "the edge" (note that "an edge" was deleted from claim 1). Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki (US 6,085,412, cited by applicants, hereinafter Iwasaki '412).

Iwasaki '412 teaches a lead frame (metal frame 12) comprising a first portion (121) spaced from a second portion (122), wherein the first portion is configured to receive an integrated circuit (11), and wherein the second portion is a conductor extending along a first plane co-planar to the first portion downward to a second plane (see figure 12) on which a surface of the conductor is adapted to releasably secure

against a receptor (a receptor, such as adaptor 90 shown in figure 15); a memory module (see figure 12) that encases the lead frame and the integrated circuit and extends to a surface co-planar with the second plane; a molded resin (20) that completely surrounds the integrated circuit and the first and second portions, except for the surface of the conductor that is adapted to releasably secure against the receptor (see figure 12 and column 7 lines 3-18); wherein the surface of the conductor extending to the second plane is exposed along an edge of the memory module (see figure 12); wherein an upper surface of the first portion is bonded to a lower surface of the integrated circuit (as shown in figure 12); wherein the conductor (122) is coupled to a bonding pad arranged upon an upper surface of the integrated circuit (the conductor 122 is coupled to a bonding pad on an upper surface of the integrated circuit via wire 14) (see figure 12, column 5 line 39 - column 6 line 4, and column 7 lines 3-18).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US 6,274,926 B1, previously cited, hereinafter Iwasaki '926) in view of the admitted prior art.

Iwasaki '926 teaches a memory module (1), comprising: a plurality of conductors (terminals 5), each of which have opposed first and second ends; an integrated circuit

(such as integrated circuit 2, for example, not specifically shown in figures 8 and 9) coupled to the first end of each of the plurality of conductors; and a molded resin (such as sealing resin 3) encasing the integrated circuit and having a first outer planar surface (not labeled, see figures 8 and 9) along which the second ends of the conductors terminate; wherein the molded resin extends at least partially around the integrated circuit to form an entire outer dimension of the memory module; wherein the entire outer dimension of the memory module is of equivalent size to a memory card (in that device 1 is a memory card itself); wherein the memory module is mechanically and electrically interchangeable with a memory card (any device 1 may be interchangeable with another device 1); further comprising wires (wires 4, for example, not specifically shown in figures 8 and 9) extending between a plurality of bonding pads (not shown) on the integrated circuit and the first end of each of the plurality of conductors; (see figures 8, 9, 1-7, and column 6 lines 64 - column 7 line 61).

Iwasaki '926 fails to specifically teach that a lateral surface of the plurality of conductors partially extend to the respective second ends that terminate in a single row substantially flush with a second outer planar surface approximately perpendicular to the first outer surface; wherein an edge of the memory module is adapted for slideable engagement into a receptor that is electrically connected to an electronic system; wherein the second end of each of the plurality of conductors are adapted for frictional engagement with, and electrical connection to, conductive elements arranged within the receptors, during times when the edge of the memory module is slid into the receptor; the entire outer dimension of the memory module except for the second end of each of

the plurality of conductors is surrounded by a covering that employs a mechanical tab which, when actuated, prevents writing data to the integrated circuit; solder extending between a plurality of bonding pads on the integrated circuit and the first end of each of the plurality of conductors; and wherein the plurality of conductors comprise flattened metal strips attributed to a tape mounted upon a Tape Automated Bonding (TAB) device.

The admitted prior art teaches that memory modules (such as card 10) were well known to those of ordinary skill in the art at the time of the invention, and are commercially available (see page 3, lines 17-19, of the specification). The memory module (card 10) includes conductors (12), a lateral surface of the plurality of conductors partially extend to the respective second ends that terminate in a single row substantially flush with a second outer planar surface (the outer planar surface of edge 14) approximately perpendicular to a first outer surface (the top or bottom of card 10, for example); wherein an edge (14) of the memory module is adapted for slideable engagement into a receptor (22) that is electrically connected to an electronic system (24); wherein the second end of each of the plurality of conductors are adapted for frictional engagement with, and electrical connection to, conductive elements (28) arranged within the receptors, during times when the edge of the memory module is slid into the receptor (see figures 1, 2, and pages 3 line 8 - page 5 line 14, of the specification); that it was well known to those of ordinary skill in the art at the time of the invention to surround the entire outer dimension of a memory module (10) except for a second end of each of a plurality of conductors (12) with a covering (36) that employs a

mechanical tab (38) which, when actuated, prevents writing data to the integrated circuit (see figure 2 and page 4 lines 4-12 of the specification); to electrically connect leads to corresponding bonding pads on an integrated circuit using a Tape Automated Bonding (TAB) device (thus, including the use of solder) (see page 2 lines 14-21 of the specification).

In view of the admitted prior art teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the system as taught by Iwasaki '926, a lateral surface of the plurality of conductors partially extend to the respective second ends that terminate in a single row substantially flush with a second outer planar surface approximately perpendicular to the first outer surface; wherein an edge of the memory module is adapted for slideable engagement into a receptor that is electrically connected to an electronic system; wherein the second end of each of the plurality of conductors are adapted for frictional engagement with, and electrical connection to, conductive elements arranged within the receptors, during times when the edge of the memory module is slid into the receptor, in order to provide compatibility with conventional memory card systems; the entire outer dimension of the memory module except for the second end of each of the plurality of conductors is surrounded by a covering that employs a mechanical tab which, when actuated, prevents writing data to the integrated circuit, in order to provide the ability to "write protect" the memory module, thereby preventing unintended changes to the data stored in the memory module; and solder extending between a plurality of bonding pads on the integrated circuit and the first end of each of the plurality of conductors; and wherein the plurality of

conductors comprise flattened metal strips attributed to a tape mounted upon a Tape Automated Bonding (TAB) device, in order to use the most efficient and advantageous connection method according to the specific cost constraints and density of the integrated circuit bonding pads of the particular application.

7. Claims 21-23, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki '926 in view of Iwasaki '412.

The teachings of Iwasaki '926 have been discussed above. Iwasaki '926 also teaches a method for forming a memory module (1), comprising: coupling an integrated circuit (2) to at least one of a plurality of conductors (5) extending in a single direction laterally from the integrated circuit; securing the plurality of conductors between a pair of mold housings (mold housings 6b, 6c, 6d, for example, not shown in figures 8 and 9; the mold 6 registers, engages, and arranges the terminals 5, see column 5 lines 8-11), each of which have a cavity (the space present within the mold before resin 3 is injected) that surrounds opposed surfaces of the integrated circuit absent any structure between the coupled integrated circuit and the pair of mold housings (Iwasaki '926 teaches that supporting pieces are only used if required (see column 5 lines 11-14), thus teaching that it is possible to mold the memory module without any supporting structure, in some situations); and inserting resin (3) between the pair of mold housings; wherein said securing comprises suspending the integrated circuit within an air-filled space formed by the cavity of each of the mold housings by clamping the plurality of conductors between the pair of mold housings a spaced distance from the cavity (see figures 3 and 4); wherein said inserting resin comprises flowing the resin in liquid form into an air-filled

space formed by the cavity of each of the mold housings and then allowing the resin to harden (see figures 3, 4, 8, 9, column 4 line 27 - column 5 line 39, and column 6 lines 64 - column 7 line 61).

Iwasaki '926 fails to specifically teach the conductors extending along two planes substantially parallel with a plane formed by the integrated circuit.

The teachings of Iwasaki '412 have been discussed above.

In view of Iwasaki '412's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the method as taught by Iwasaki '926, the conductors extending along two planes substantially parallel with a plane formed by the integrated circuit, in order to provide added strength and simpler manufacturing steps (see column 7 lines 3-18, of Iwasaki '412).

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(ă) as being unpatentable over Iwasaki '926 as modified by the admitted prior art in view of Eguchi et al (US 2003/0071348 A1, previously cited).

The teachings of Iwasaki '926 as modified by the admitted prior art have been discussed above.

Iwasaki '926 as modified by the admitted prior art fails to specifically teach a surface of the integrated circuit is bonded to a surface of a conductive plate, the opposite surface of the conductive plate extends flush with or beyond the outer dimension of the memory module; wherein the plate is thermally conductive.

Eguchi et al teaches a semiconductor module (see figures 1A and 1B) having an integrated circuit (1) wherein a surface of the integrated circuit is bonded (via resin 5) to

a surface of a thermally conductive plate (4), the opposite surface of the conductive plate extends flush with or beyond the outer dimension of the memory module (see figures 1A, 1B, paragraphs 35, 38, and 53).

In view of Eguchi et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the system as taught by Iwasaki '926 as modified by the admitted prior art, a surface of the integrated circuit is bonded to a surface of a conductive plate, the opposite surface of the conductive plate extends flush with or beyond the outer dimension of the memory module; wherein the plate is thermally conductive, in order to help dissipate heat from the memory module, thereby helping to increase the reliability and lifespan of the memory module.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki '926 as modified by the admitted prior art as modified by Gray (US 6,367,017 B1, previously cited).

The teachings of Iwasaki '926 as modified by the admitted prior art have been discussed above.

Iwasaki '926 as modified by the admitted prior art fails to specifically teach the integrated circuit comprising memory and a memory controller embodied upon a single monolithic silicon substrate.

Gray teaches a memory card comprising a memory and a memory controller embodied on a single chip (see figure 8A and column 13 lines 15-19).

In view of Gray's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the system as taught by Iwasaki '926

as modified by the admitted prior art, the integrated circuit comprising memory and a memory controller embodied upon a single monolithic silicon substrate, in order to reduce the size of the memory module.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki '926 as modified by the admitted prior art in view of Nishizawa et al (US 6,431,456 B2, previously cited).

The teachings of Iwasaki '926 as modified by the admitted prior art have been discussed above.

Iwasaki '926 as modified by the admitted prior art fails to specifically teach a second integrated circuit stacked upon and bonded to the integrated circuit.

Nishizawa et al teaches a memory module having a second integrated circuit (34b) stacked upon and bonded to (via resin 55) a first integrated circuit (34a) (see figures 5, 6, column 14 line 65 - column 15 line 16, and column 15 lines 63-65).

In view of Nishizawa et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the system as taught by Iwasaki '926 as modified by the admitted prior art, a second integrated circuit stacked upon and bonded to the integrated circuit, in order to reduce the distances from the integrated circuits to a controller chip, as compared to the integrated circuits not being stacked (see column 15 lines 4-8, of Nishizawa et al).

11. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki '926 as modified by Iwasaki '412 in view of Nishizawa et al (US 6,431,456 B2, previously cited).

The teachings of Iwasaki '926 as modified by Iwasaki '412 have been discussed above.

Iwasaki '926 as modified by Iwasaki '412 fails to specifically teach a second integrated circuit stacked upon and bonded to the integrated circuit.

Nishizawa et al teaches a memory module having a second integrated circuit (34b) stacked upon and bonded to (via resin 55) a first integrated circuit (34a) (see figures 5, 6, column 14 line 65 - column 15 line 16, and column 15 lines 63-65).

In view of Nishizawa et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the system and method as taught by Iwasaki '926 as modified by Iwasaki '412, a second integrated circuit stacked upon and bonded to the integrated circuit, in order to reduce the distances from the integrated circuits to a controller chip, as compared to the integrated circuits not being stacked (see column 15 lines 4-8, of Nishizawa et al).

Response to Arguments

12. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection. Please note that different embodiments of some of the references have now been applied. For example, the embodiment shown in figures 8 and 9 of Iwasaki '926, which teaches exposed external conductors, and the embodiment shown in figure 12 of Iwasaki '412, which teaches a lead frame having a first portion spaced apart from a second portion, wherein the second portion is a conductor extending along a first plane co-planar to the first portion downward to a second plane.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Arndt (US 2003/0189236 A1), Tsubosaki et al (US 6,664,616 B2), Ohki (US 6,143,590) and Ohki (US 5,886,408) all teach memory modules. Yamawaki et al (US 4,894,707) teaches a method for forming a module including clamping conductors between mold housings (see figure 3b).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared J. Fureman whose telephone number is (571) 272-2391. The examiner can normally be reached on 7:00 am - 4:30 PM M-T, and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jared J. Fureman
Examiner
Art Unit 2876

March 22, 2004